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Mahdi Nikdast

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Education

Ph.D. **Hong Kong University of Science and Technology (HKUST)** 2009-2014

Electronic and Computer Engineering

Ph.D. Thesis: Signal-to-noise Ratio (SNR) in Optical Interconnection Networks: Analysis, Modeling, and Comparison

Advisor: Prof. Jiang Xu

B.Sc. **Najafabad Azad University (Iran)** 2005-2009

Computer Science and Engineering

Thesis: Parameterized Intermittent Routing Algorithm for Networks-on-Chip

CGPA: 4.0 / 4.0

Ranking: 1/200

Current Position

Postdoctoral Fellow **Polytechnique Montréal** Sep. 2014-Present

(In collaboration with McGill University)

Computer and Software Engineering Department

Montréal, Canada

Research Experience

Postdoctoral Research **Polytechnique Montréal (In collaboration with McGill University)** 2014-Present

Computer and Software Engineering Department

Montréal, Canada

Laboratory: Heterogeneous Embedded System Lab (HESL)

Project 1: Reliability and Variability of Multiprocessor Computing Systems Employing Optical Interconnection Networks (OINs)

Project 2: Design, Fabrication, and Characterization of Silicon Photonic Devices and Integrated Circuits

Doctoral Research **Hong Kong University of Science and Technology** 2009- 2014

Electronic and Computer Engineering Department

Hong Kong

Laboratory: Mobile computing System Lab

Project: Crosstalk Noise Analysis in MPSoCs Integrating Optical Interconnection Networks

Honors and Awards

Best Paper Award	♦ **Best Paper Award, Test and Robustness Track** Design, Automation, and Test in Europe **(DATE)** Conference, Dresden, Germany	2016
	♦ **Best Paper Award, The Optical Society (OSA)** Asia Communications and Photonics Conference **(ACP)** IEEE Photonics and Optical Society, Hong Kong	2015
	♦ **Second Best Project Award** AMD Technical Forum and Exhibition **(AMD-TFE)** Taipei, Taiwan	2010
Fellowship and Scholarship	♦ NSERC CREATE Postdoctoral Fellowship (SiEPIC Program), Canada	2015-2017
	♦ ReSMiQ Postdoctoral Fellowship, Canada	2014
	♦ School of Engineering Ph.D. Fellowship For Outstanding Students, HKUST, Hong Kong	2012-2013
	♦ Postgraduate Scholarship, Electronic and Computer Engineering Department, HKUST, Hong Kong	2009-2013
	♦ Outstanding Student Scholarship, Computer Engineering Department, Najafabad Azad University, Esfahan, Iran	2006-2009
Travel Grant	♦ Design Automation Conference (DAC), Austin, USA	2016
	♦ Design, Automation, and Test in Europe (DATE) Conference, Grenoble, France	2015
	♦ Design Automation Conference (DAC), San Francisco, USA	2014
	♦ AMD Technical Forum and Exhibition, Taipei, Taiwan	2010

Supervisory Experience

Advisor on Graduate Projects	♦ Multi-Objective Optimization in the Design of Embedded Systems HESL, Polytechnique Montréal, Canada	2016-Present
	♦ Low-Latency Electronic Controllers for Photonic Switched Networks McGill University and Polytechnique Montréal, Canada	2014-Present
	♦ Coherent Crosstalk Noise and SNR Analyses in Ring-Based ONoCs Mobile Computing System Lab, HKUST, Hong Kong	2013-2014
Advisor on Undergraduate Final Projects	♦ Network-level Simulator for Optical Networks-on-Chip Electronic and Computer Engineering Department, HKUST	2010-2011

- Optical Router Power Loss Analysis Simulator — 2009-2010
  Electronic and Computer Engineering Department, HKUST

Teaching Experience

Instructor

Departmental Seminar — April 2016-March 2017
Computer and Software Engineering Department
Polytechnique Montréal, Canada

Teaching Assistant

Embedded System Design — 2010-2014
Electronic and Computer Engineering Department
HKUST, Hong Kong

Course Assistant

Computer Architecture — 2007-2008
Computer Engineering Department
Najafabad Azad University, Iran

Digital Design — 2007-2008
Computer Engineering Department
Najafabad Azad University, Iran

Professional Memberships, Service and Activities

Memberships

- IEEE Member — 2013-Present
- IEEE Graduate Student member — 2010-2013

Research Grant Proposal

- Natural Sciences and Engineering Research Council (NSERC) — 2015-2017
  Canada
  Funded project: On the Impact of Fabrication Process Variations in Photonic Integrated Circuits
  Acceptance rate: 25%, Amount: CAD40,000
- Regroupement Strategique en MicroSystemes du Quebec (ReSMiQ) — 2015
  Quebec, Canada
  Funded project: From Metallic to Photonic Interconnect: Paving the Way for High-Performance Computing Systems
  Acceptance rate: 30%, Amount: CAD20,000

Research Grant Proposal (Contributed)

- Natural Sciences and Engineering Research Council (NSERC) — 2014-Present
  Canada
  Funded project: System-Level Modeling and Analysis of 3D Multi-Processors on Chip for Future Cloud Computing
  Acceptance rate: 30%, Amount: CAD130,000
- The Research Grant Council (RGC) — 2010-2014
  Hong Kong

Organizing Committee

- Ph.D. Forum Chair at The Eights International Green and Sustainable Computing Conference (Ph.D. Forum at IGSC'17) — 2017
  IGSC 2017, Orlando, USA
- The 3rd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS) **(Founder and Program Chair)** — 2017
  DATE 2017, Lausanne, Switzerland
- The 2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS) **(Founder and Program Chair)** — 2016
  DATE 2016, Dresden, Germany
- The 1st International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS) **(Founder and Program Chair)** — 2015
  DATE 2015, Grenoble, France
- Special Session on Silicon Photonics Interconnect Networks (Co-organizer) — 2014
  NOCS 2014, Ferrara, Italy

Journal Reviewer (Most recent ones)

- IEEE Transactions on VLSI Systems *(IEEE TVLSI)*
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (*IEEE TCAD)*
- IEEE Design and Test of Computers *(IEEE D&T)*
- IEEE Transactions on Parallel and Distributed Systems *(IEEE TPDS)*
- IEEE Transactions on Emerging Topics in Computing *(IEEE TETC)*
- IEEE Transactions on Multi-Scale Computing Systems *(IEEE TMSCS)*
- ACM Transactions in Embedded Computing Systems *(ACM TECS)*
- ACM Journal of Emerging Technologies in Computing Systems *(ACM JETC)*
- Elsevier Journal of Systems Architecture *(JSA)*
- IEEE Journal of Lightwave Technology *(IEEE JLT)*
- IEEE Photonics Technology Letters

Conference Reviewer (Most recent ones)

- IEEE/ACM Design Automation Conference *(DAC)*
- International Symposium on Networks-on-Chip *(NoCs)*
- IEEE/ACM International Conference on Computer-Aided Design *(ICCAD)*

Invited Talks

- **Multiprocessor Computing Systems Integrating Silicon Photonic Interconnects** — April 2017
  Ingram School of Engineering
  Texas State University, Saint Marcos, US

- **Multiprocessor Computing Systems Integrating Silicon Photonic Interconnects** — February 2017
  Electrical and Computer Engineering Department
  Colorado State University, Fort Collins, US

- **Silicon Photonic Interconnection Networks for Multiprocessor Computing Systems: Let's Meet in the Middle!** — November 2016
  Electrical and Computer Engineering Department
  University of Toronto, Toronto, Canada

- **Enabling Tolerance Analysis in Silicon Photonic Integrated Circuits** — August 2016
  Progress in Electromagnetics Research Symposium (PIERS)
  Special Session on Nanophotonics and Integration
  Shanghai, China

- **An Analytical Study of Process Variations in Silicon Photonics Integrated Circuits** — May 2016
  Photonics North Conference
  Photonics Theory, Simulation and Design Session
  Quebec City, Canada

- **Fabrication Non-Uniformity in Silicon Photonic Interconnects** — March 2016
  Optical/Photonic Interconnects for Computing Systems (OPTICS) Workshop
  Dresden, Germany

- **CLAP: a Crosstalk and Loss Analysis Platform for Optical Interconnects** — September 2014
  IEEE/ACM International Symposium on Networks-on-Chip (NoCs)
  Special Session on Silicon Photonic Interconnects
  Ferrara, Italy

- **Formal Worst-case Analysis of Crosstalk Noise in Mesh-based Optical Networks-on-Chip** — October 2012
  Networks-on-Chip Workshop
  HKUST, Hong Kong

- **A Formal Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip for Chip Multiprocessors** — October 2010
  AMD Technical Forum and Exhibition
  Taipei, Taiwan

- **Bit Error Rate Analysis in Optical Networks-on-Chip** — July 2010
  University of Tehran (UT)
  School of Electrical and Computer Engineering, UT, Tehran, Iran

Professional Development

Research Related

DAC Young Faculty Workshop *(Workshop)* — Summer 2016
Design Automation Conference (DAC), Austin, USA

Clarifying Expectations for Supervision *(Workshop)* — Winter 2016
McGill University, Montréal, Canada

Crafting Your Research Future *(Workshop)* — Spring 2013
Center for Enhanced Learning and Teaching, HKUST, Hong Kong

Modern Engineering Research Methodology *(Graduate course)* — Spring 2012
Electronic and Computer Engineering Department, HKUST, Hong Kong

Effective Research Process *(Graduate course)* — Spring 2011
Electronic and Computer Engineering Department, HKUST, Hong Kong

Teaching Related

Prepare For an Academic Career *(Graduate course)* — Spring 2013
Center for Enhanced Learning and Teaching, HKUST, Hong Kong

Teaching Preparation For Graduate Teaching Assistants *(Workshop)* — August 2010
Center for Enhanced Learning and Teaching, HKUST, Hong Kong

Publications and Presentations

Book

[1]. **M. Nikdast**, G. Nicolescu, S. Le Beux, and J. Xu, "Photonic Interconnects for Computing Systems," *to be published by River Publishers*, 2017.

Book Chapters

[2]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Improving Reliability in Nanophotonic Networks-on-Chip," *Photonics Interconnects for Computing Systems,* River Publishers, 2017.

[3]. Felipe Gohring, **Mahdi Nikdast**, Fabiano Hessel, Odile Liboiron-Ladouceur, and Gabriela Nicolescu, "Optical Interconnection Networks: The Need for Low-Latency Controllers," *Photonic Interconnects for Computing Systems,* River Publishers, 2017.

Refereed Journal Publications

[4]. R. Ayari, **M. Nikdast**, and G. Nicolescu, "HypAp: a Hypervolume-Based Approach for Refining the Design of Embedded Systems," *accepted by IEEE Embedded Systems Letters,* 2017.

[5]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Chip-Scale Silicon Photonic Interconnects: a Formal Study on Fabrication Non-Uniformity," *IEEE Journal of Lightwave Technology (IEEE JLT),* vol. 32, no. 16, pp. 3682-3695, August 2016.

[6]. L. H. K. Duong, Z. Wang, **M. Nikdast**, J. Xu, P. Yang, Zh. Wang, R. Maeda, H. Li, X. Wang, S. Le Beux, and Y. Thonnart, "Coherent and Incoherent Crosstalk Noise Analyses in Inter/Intra-chip Optical Interconnection Networks," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol. 24, no. 7, pp. 2475-2487, July 2016.

[7]. F. Gohring, R. Priti, **M. Nikdast**, F. Hessel, O. Liboiron-Ladouceur, and G.

Nicolescu, "Design and Modelling of a Low-Latency Centralized Controller for Optical Integrated Networks," *IEEE Communications Letters (IEEE COMML)*, vol. 20, no. 3, pp. 462-465, March 2016.

[8]. **M. Nikdast**, J. Xu, X. Wu, X. Wang, Z. Wang, Zh. Wang, and P. Yang, "Crosstalk Noise in WDM-based Optical Networks-on-Chip: a Formal Study and Comparison," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI),* vol. 23, no. 11, pp. 2552-2565, November 2015.

[9]. X. Wu, J. Xu, Y. Ye, X. Wang, **M. Nikdast**, Z. Wang, and Zh. Wang, "An Inter/Intra-chip Optical Network for Manycore Processors," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol.23, no. 4, pp. 678-691, April 2015.

[10]. X. Wang, J. Xu, W. Zhang, X. Wu, Y. Ye, Z. Wang, **M. Nikdast**, and Zh. Wang, "Actively Alleviate Power-Gating-Induced Power/Ground Noise Using Parasitic Capacitance of On-Chip Memories in MPSoCs," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol. 23, no. 2, pp. 266-279, February 2015.

[11]. **M. Nikdast**, J. Xu, L. H. K. Duong, X. Wu, Z. Wang, X. Wang, and Zh. Wang, "Fat-Tree-Based Optical Interconnection Networks Under Crosstalk Noise Constraint," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol.23, no.1, pp. 156-169, January 2015.

[12]. Y. Ye, Z. Wang, J. Xu, X. Wu, X. Wang, **M. Nikdast**, Zh. Wang, and L. H. K. Duong, "System-Level Modeling and Analysis of Thermal Effects in WDM-Based Optical Networks-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, vol.33, no. 11, pp. 1718-1731, November 2014.

[13]. L. H. K. Duong, **M. Nikdast**, S. Le Beux, J. Xu, X. Wu, Z. Wang, P. Yang, "A Case Study of Signal-to-Noise Ratio in Ring-Based Optical Networks-on-Chip," *IEEE Design and Test of Computers (IEEE D&T)*, vol.31, no. 5, pp. 55-65, October 2014.

[14]. X. Wu, J. Xu, Y. Ye, Z. Wang, **M. Nikdast**, and X. Wang, "SUOR: Sectioned Undirectional Optical Ring for Chip Multiprocessor," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, vol. 10, no. 4, pp. 1-25, June 2014.

[15]. Z. Wang, J. Xu, X. Wu, Y. Ye, W. Zhang, **M. Nikdast**, X. Wang, and Zh. Wang, "Floorplan Optimization of Fat-Tree Based Networks-on-Chip for Chip Multiprocessors," *IEEE Transactions on Computers (IEEE TC)*, vol. 63, no. 6, pp. 1446-1459, June 2014.

[16]. X. Wu, Y. Ye, J. Xu, W. Zhang, W. Liu, **M. Nikdast**, and X. Wang, "UNION: a Unified Inter/Intra-Chip Optical Network for Chip Multiprocessors," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol. 22, no. 5, pp. 1082-1095, May 2014.

[17]. **M. Nikdast**, J. Xu, X. Wu, W. Zhang, Y. Ye, X. Wang, Z. Wang, and Zh. Wang, "Systematic Analysis of Crosstalk Noise in Folded-Torus-Based Optical Networks-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and*

Systems (IEEE TCAD), vol. 33, no. 3, pp. 437-450, March 2014.

[18]. W. Liu, X. Wang, J. Xu, W. Zhang, Y. Ye, X. Wu, **M. Nikdast**, and Z. Wang, "On-Chip Sensor Networks for Soft-Error Tolerant Real-Time Multiprocessor Systems-on-Chip," *ACM Journal of Emerging Technologies in Computing Systems (ACM JETC)*, vol. 10, no. 2, pp. 1-20, March 2014.

[19]. Y. Xie, **M. Nikdast**, J. Xu, X. Wu, W. Zhang, Y. Ye, X. Wang, Z. Wang, and W. Liu, "A Formal Worst-Case Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol. 21, no. 10, pp. 1823-1836, October 2013.

[20]. Y. Ye, J. Xu, B. Huang, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, W. Liu, and Zh. Wang, "3D Mesh-based Optical Network-on-Chip for Multiprocessor System-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, vol. 32, no. 4, pp. 584-596, April 2013.

[21]. Y. Ye, J. Xu, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, and W. Liu, "System-Level Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip," *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, vol. 21, no. 2, pp. 292-305, February 2013.

[22]. Y. Ye, J. Xu, X. Wu, W. Zhang, W. Liu, and **M. Nikdast**, "A Torus-based Hierarchical Optical-Electronic Network-on-Chip for Multiprocessor System-on-Chip," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, vol. 8, no. 1, pp. 1-26, February 2012.

IEEE Potentials Magazine

[23]. **M. Nikdast**, "Research Papers: Writing Tips and Top-Tier Targets," *IEEE Potentials*, vol. 36, no. 3, pp. 26-29, May-June 2017.

[24]. **M. Nikdast**, "Research Tips for Frist-Year Ph.D. Students," *IEEE Potentials*, vol. 35, no. 3, pp. 18-20, May-June 2016.

[25]. Sh. Sinha and **M. Nikdast**, "Finding Happiness and Satisfaction during Your Ph.D. Program," *IEEE Potentials*, vol. 34, no. 3, pp. 36-38, May-June 2015.

Refereed Conference Publications

[26]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Enabling Efficient Tolerance Analysis in Silicon Photonic Integrated Circuits," in *Proc. Progress in Electromagnetic Research Symposium (PIERS)*, Shanghai, China, August 2016. **(Invited)**

[27]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "An Analytical Study of Process Variations in Silicon Photonic Integrated Circuits," in *Proc. Photonics North Conference (PN)*, Quebec City, Canada, May 2016. **(Invited)**

[28]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Modeling Fabrication Non-Uniformity in Chip-Scale Silicon Photonic Interconnects," in *Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Germany, March 2016. **(Best Paper Award, Test Track)**

[29]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Photonic Integrated Circuits: a Study on Process Variations," in *Proc. Optical Fiber Communication Conference and Exhibition (OFC)*, USA, March 2016.

[30]. **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Silicon Photonic Integrated Circuits under Process Variations," in *Proc. Asia Communications and Photonics Conference (ACP)*, Hong Kong, November 2015. **(Best Paper Award)**

[31]. F. Gohring, R. Priti, **M. Nikdast**, F. Hessel, O. Liboiron-Ladouceur, and G. Nicolescu, "A Low-Latency Centralized Controller for MZI-based Optical Integrated Networks," *Photonics Switching Conference (PS)*, Italy, September 2015.

[32]. L. H. K. Duong, **M. Nikdast**, J. Xu, Z. Wang, Y. Thonnart, S. Le Beux, P. Yang, X. Wu, and Zh. Wang, "Coherent Crosstalk Noise Analyses in Ring-based Optical Interconnects," in *Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE),* France, March 2015.

[33]. **M. Nikdast**, L. H. K. Duong, J. Xu, S. Le Beux, X. Wu, Z. Wang, P. Yang, and Y. Ye, "CLAP: a Crosstalk and Loss Analysis Platform for Optical Interconnects," in *Proc. IEEE/ACM International Symposium on Networks-on-Chip (NOCS),* Italy, September 2014.

[34]. Y. Ye, X. Wu, J. Xu, **M. Nikdast**, Z. Wang, and X. Wang, "System-level Analysis of Mesh-based Hybrid Optical-Electronic Network-on-Chip," *IEEE International Symposium on Circuits and Systems (ISCAS)*, China, May 2013. **(Invited)**

[35]. X. Wang, J. Xu, W. Zhang, X. Wu, Y. Ye, Z. Wang, **M. Nikdast**, and Zh. Wang, "Active Power-Gating-Induced Power/Ground Noise Alleviation Using Parasitic Capacitance of On-Chip Memories," in *Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 1221-1224, France, March 2013.

[36]. W. Liu, Z. Wang, X. Wu, J. Xu, B. Li, W. Zhang, Y. Ye, Z. Wang, and **M. Nikdast**, "An Network-on-Chip Benchmark Suite based on Real Applications," *in Proc. Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, China, February 2013. **(Invited)**

[37]. Y. Ye, X. Wu, J. Xu, W. Zhang, **M. Nikdast**, and X. Wang, "Holistic Comparison of Optical Routers for Chip Multiprocessors," in *Proc. IEEE International Conference on Anti-Counterfeiting, Security and Identification (ASID)*, pp. 1-5, Taiwan, August 2012. (**Invited**)

[38]. Y. Ye, J. Xu, X. Wu, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, Z. Wang, and Zh. Wang, "Thermal Analysis for 3D Optical Network-on-Chip Based on a Novel Low-Cost 6×6 Optical Router," in *Proc. IEEE Optical Interconnects Conference (OI-Conference)*, pp. 110-111, USA, May 2012.

[39]. Z. Wang, J. Xu, X. Wu, Y. Ye, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, and Zh. Wang, "A Novel Low-Waveguide-Crossing Floorplan for Fat Tree Based Optical Networks-on-Chip," in *Proc. IEEE Optical Interconnects Conference (OI-*

Conference), pp. 100-101, USA, May 2012.

[40]. Y. Ye, J. Xu, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, and W. Liu, "Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 254-259, India, July 2011.

[41]. W. Liu, J. Xu, X. Wu, Y. Ye, X. Wang, W. Zhang, **M. Nikdast**, Z. Wang, "A NoC Traffic Suite Based on Real Applications," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 66-71, India, July 2011.

[42]. W. Liu, J. Xu, X. Wang, Y. Wang, W. Zhang, Y. Ye, X. Wu, **M. Nikdast**, and Z. Wang, "A Hardware-Software Collaborated Method for Soft-Error Tolerant MPSoC," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 260-265, USA, July 2011.

[43]. Y. Xie, **M. Nikdast**, J. Xu, W. Zhang, Q. Li, X. Wu, Y. Ye, W. Liu, and X. Wang, "Crosstalk Noise and Bit Error Rate Analysis for Optical Networks-on-Chip," in *Proc. Design Automation Conference (DAC)*, pp. 657-660, USA, June 2010. (Acceptance rate: 24%)

[44]. X. Wu, Y. Ye, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, and J. Xu, "UNION: A Unified Inter/Intra-Chip Optical Network for Chip Multiprocessors," in *Proc. IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, pp. 35-40, USA, June 2010. (**Invited**).

[45]. S. Nasrolahi and **M. Nikdast**, "The Semantic Web: A New Approach for Future World Wide Web," *International Conference of Information Technology (ICIT)*, Italy, October 2009.

[46]. H. Ahmadi and **M. Nikdast**, "Age-Based Adaptive Routing Algorithm for Network-on-Chip," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Iran, August 2009.

[47]. M. Davarpanah, A. Mohamad Shafiee, **M. Nikdast**, and M. Montazeri, "A Predetermined Routing Algorithm for Network-on-Chip," *Iranian Conference on Electrical Engineering (ICEE)*, Iran, May 2009. (Acceptance rate: 21%)

[48]. A. M. Shafiee, **M. Nikdast**, and M. Montazeri, "Parameterized Intermittent Routing Algorithm in Networks-on-Chip," *IEEE International Conference on Emerging Trends in Computing (ICETiC)*, India, January 2009.

[49]. A. M. Shafiee, M. Montazeri, and **M. Nikdast**, "An Innovational Intermittent Routing Algorithm in Network-on-Chip," *International Conference on Computer Science and Engineering (ICCSE)*, France, September 2008.

[50]. B. Soleimani, E. Shahabian, M. yavari, and **M. Nikdast**, "A Novel Heuristic for Solving the 8 Puzzle Problem Based on IDA Method," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Iran, August 2008.

Refereed Conference Poster Presentations

[51]. **M. Nikdast**, "Optical Interconnects for Computing Systems: a Formal Study on Signal-to-Noise Ratio, "*Design, Automation and Test in Europe Conference and Exhibition (DATE),* France, March 2015. (*Ph.D. Forum)*

[52]. **M. Nikdast** and J. Xu, "On the Impact of Crosstalk Noise in Optical Networks-on-Chip," *Design Automation Conference (DAC)*, USA, June 2014. (*Poster,* Acceptance rate: 30%)

[53]. Z. Wang, J. Xu, X. Wu, X. Wang, Zh. Wang, **M. Nikdast**, P. Yang, "Holistic Modeling and Comparison of Inter-Chip Optical and Electrical Interconnects," Design Automation Conference *(DAC)*, June 2014. (*Poster*)

[54]. W. Liu, J. Xu, X. Wu, Y. Ye, X. W., W. Zhang, **M. Nikdast**, and Z. Wang, "MCSL: A Realistic Traffic Benchmark Suite for Network-on-Chip Studies," *Design Automation Conference (DAC)*, USA, June 2011. *(Poster)*

[55]. W. Liu, J. Xu, X. Wang, Y. Wang, W. Zhang, Y. Ye, X. Wu, **M. Nikdast**, and Z. Wang, "A Low-Overhead Hardware-Software Collaborated Approach for Soft-Error Tolerance," *Design Automation Conference (DAC)*, USA, June 2011. *(Poster)*

[56]. **M. Nikdast**, J. Xu, X. Wu, Y. Ye, W. Liu, and X. Wang, "A Formal Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip for Chip Multiprocessors," *AMD Technical Forum and Exhibition (AMD-TFE)*, Taiwan, October 2010. **(Best Project Award, Second place)**

[57]. W. Liu, X. Wang, J. Xu, X. Wu, Y. Ye, and **M. Nikdast**, "A Case Study of On-Chip Sensor Networks for Soft-Error Tolerant Multiprocessor Systems-on-Chip," *AMD Technical Forum and Exhibition (AMD-TFE)*, Taiwan, October 2010. **(Invited poster)**

[58]. **M. Nikdast** and M. Montazeri, "Analysis of Different Routing Algorithms in NoCs," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Iran, August 2008. *(Poster)*